

# ESD Protection for CMOS Output Buffer by Using Modified LVTSCR Devices with High Trigger Current

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**Abstract**—Modified designs of the low-voltage triggering semiconductor-controlled rectifier (LVTSCR) devices with high trigger current are proposed to protect the CMOS output buffer against electrostatic discharge (ESD) events in submicrometer CMOS technologies. The high trigger current is achieved by inserting the bypass diodes into the structures of the modified PMOS-trigger lateral SCR (PTLSCR) and NMOS-trigger lateral SCR (NTLSCR) devices. These modified PTLSCR and NTLSCR devices have a lower trigger voltage to effectively protect the output transistors in the ESD-stress conditions, but they also have a higher trigger current to avoid the accidental triggering due to the electrical noise on the output pad in the normal operating conditions of CMOS IC's. Experimental results have verified that the trigger current of the modified PTLSCR (NTLSCR) is increased up to 225.5 mA (218.5 mA). The noise margin to the overshooting (undershooting) voltage pulse on the output pad, without accidentally triggering on the modified NTLSCR (PTLSCR), is more than  $V_{DD} + 12$  V ( $V_{SS} - 12$  V).

**Index Terms**—ESD, latchup, LVTSCR, noise margin.

## I. INTRODUCTION

ELECTROSTATIC discharge (ESD) protection has become a main concern on the reliability of IC products in submicrometer CMOS technologies. Especially, the drains of NMOS and PMOS devices in the CMOS output buffer are often directly connected to the output pad to drive the external load, so the CMOS output buffer is more vulnerable to ESD stress. To improve ESD robustness of a CMOS output buffer and also to drive/sink current to/from the external heavy load, the output NMOS and PMOS devices are often designed with large device dimensions. Even with such large device dimensions, the ESD robustness of the CMOS output buffer had been reported to be seriously degraded by the advanced submicrometer CMOS technologies [1]–[4].

Recently, the lateral semiconductor-controlled rectifier (SCR) device had been used as an ESD-protection element for input protection in submicrometer CMOS IC's [5]–[8]. To effectively protect the CMOS output buffer, the low-voltage triggering SCR (LVTSCR) device has been invented with a much lower trigger voltage [9]–[12]. The trigger voltage of the LVTSCR device is equivalent to the snapback-trigger voltage of the short-channel NMOS (or PMOS) device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30–50 V) of the lateral SCR device. To protect the output transistors in the CMOS output buffer, the inserted NMOS (or PMOS) in the LVTSCR should be designed with a shorter channel length than the output NMOS

(PMOS) in the CMOS output buffer [9]–[12]. But with such a low trigger voltage of the LVTSCR, the corresponding trigger current of the PMOS-trigger lateral SCR (PTLSCR) and NMOS-trigger lateral SCR (NTLSCR) are only about 4.7 mA and 12.3 mA in a 0.6- $\mu$ m CMOS technology, respectively [11]. The lower trigger voltage of the PTLSCR and NTLSCR can provide effective ESD protection for the CMOS output buffer, but the lower trigger current may cause the PTLSCR and NTLSCR to be accidentally triggered on by the external overshooting or undershooting noise pulses on the output pin while the CMOS IC is in its normal operating condition.

In this paper, a modified PTLSCR and a modified NTLSCR with lower trigger voltage but higher trigger current are proposed to safely protect the CMOS output buffer without being accidentally triggered on by the electrical noisy pulse when the CMOS IC's are in the normal operating conditions.

## II. MODIFIED PTLSCR/NTLSCR DEVICES WITH HIGH TRIGGER CURRENT

### A. Modified Device Designs

The schematic cross-sectional views of the modified PTLSCR and NTLSCR in a P-substrate N-well CMOS process are shown in Fig. 1(a) and (b), respectively. The modified PTLSCR is formed by inserting a bypass diode Dn2 into the PTLSCR structure as shown in Fig. 1(a). The modified NTLSCR is formed by inserting a bypass diode Dp2 into the NTLSCR structure as shown in Fig. 1(b). The Dn2 (Dp2) is located into the latching path of the PTLSCR (NTLSCR). This Dn2 (Dp2) has an effect of reducing the equivalent substrate resistor Rsub1 (N-well resistor Rnw2) and an effect of bypassing the latchup trigger current in the P-substrate (the N-well), so the trigger current to initiate the positive-feedback regenerative process of latchup in the PTLSCR (NTLSCR) can be significantly increased [13]–[14]. So, by adding this bypass diode Dn2 (Dp2), the trigger current of the modified PTLSCR (modified NTLSCR) can be significantly increased to avoid the accidental triggering by the external noisy pulse. The trigger voltage of this modified PTLSCR (modified NTLSCR) is still kept the same as the snapback-trigger voltage of the short-channel PMOS (NMOS) which is inserted in the PTLSCR (NTLSCR) structure [11]. This modified PTLSCR (modified NTLSCR) can be merged with the output PMOS (NMOS) in the layout to save layout area as shown in Fig. 1(a) and (b).

Since ESD voltages may have positive or negative polarities on a pin to either the VDD or the VSS pins, there are four different ESD-stress conditions on an output pin. The four ESD-stress conditions on a pin have been specified as PS, NS, PD, and ND modes in [12]. In the CMOS output buffers, there also exist two parasitic junction diodes, Dp1

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# Kssats Papers 1997

**John L. Fize**



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