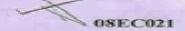
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M.Tech. Degree Examination, Dec.09/Jan.10 **CMOS VLSI Design**

TOTAL	The same	hrs. Max. M	arks:100
		Note: Answer any FIVE full questions.	
1	- a.	With neat sketches, explain the behaviour of nMOS device under the influence	of different
		terminal voltages (Enhancement mode).	(09 Marks)
	b.	Explain small signal model for an MOS transistor.	(66 Marks)
	C.	Write a note on differential inverter.	(05 Marks)
2	10.0	Explain λ based design rules.	(08 Marks)
	b.	Obtain the scaling factors for the following:	
		i) Gate capacitance C _g	
		ii) Saturation current lass	
		iii) Parasitic capacitance.	(06 Marks)
	C.	Define sheet resistance and also explain the concept applied to MOS transistor an	(06 Marks)
3	20.	Explain the second order effects associated with a MOSFET.	(10 Marks)
	Ь.	Explain twin tub CMOS process.	(10 Marks)
4	a.	Explain the effect of long polysilicon wires. Show how to improve the signal prop	regation.
	b	Derive the threshold voltage equation (V ₁) for 2 inputs CMOS NOR gate (V _{1 NOR2})	
	6.	For the given function $f = \overline{AB} + A\overline{C} + A(B + D)$, obtain	orders to the state of the
	-		
		i) CMOS TG realization	
		ii) CMOS transistor realisation	(06 Marks)
5	n.	Explain the function of D latch with gate level schematic and CMOS circuit.	(06 Marks)
	25.	Explain synchronous dynamic circuit implemented using depletion load nMOS.	(99 Marks)
	C.	Explain the principle of pass transistor circuit.	(05 Marks)
6	28	Discuss the general principle of band gap reference and hence obtain expression f	or V _{EE} .
	to.	Explain cross operational amplifier with necessary expression and characteristics.	
	-6.	Mention the advantages of CMOS over NMOS.	(04 Marks)
	1000		And send they
7	12.	Describe different clock distribution schemes.	(06 Marks)
	100	Mention the causes of latch up and guidelines for avoiding latch up.	(10 Marks)
	C.	Realize the following function Z = AB + (C + D) (E + F) + GH using i) Standard CMOS	
		i) Standard CMOS ii) Domino CMOS.	(04 Marks)
		ii) Dollinio Civios.	(04 NEATHO)
8		Write short notes on:	
	The case of		
		Dynamic CMOS logic	
	0.	Voltage boot strapping	Carrier Statement
	4.	Current mirror.	(20 Marks)

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