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Minimizing and Exploiting Leakage in VLSI Design

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Minimizing And Exploiting Leakage In Vlsi Design

**Stamatis Vassiliadis, Stephan
Wong, Timo D. Härmäläinen**



Minimizing And Exploiting Leakage In Vlsi Design:

Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar, Suganth Paul, Rajesh Garg, 2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate. This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today. Traditionally dynamic switching power has dominated the total power consumption of an IC. However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits. Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs. This book presents two techniques aimed at reducing leakage power in digital VLSI ICs. The first technique reduces leakage through the selective use of high threshold voltage sleep transistors. The second technique reduces leakage by applying the optimal Reverse Body Bias (RBB) voltage. This book also shows readers how to turn the leakage problem into an opportunity through the use of sub threshold logic.

Minimizing and Exploiting Leakage in VLSI Nikhil Jayakumar, 2010 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate. This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today. Traditionally dynamic switching power has dominated the total power consumption of VLSI circuits. However due to process scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits. This dissertation explores techniques to reduce leakage as well as techniques to exploit leakage currents through the use of sub threshold circuits. This dissertation consists of two studies. In the first study techniques to reduce leakage are presented. These include a low leakage ASIC design methodology that uses high V_T sleep transistors selectively, a methodology that combines input vector control and circuit modification, and a scheme to find the optimum reverse body bias voltage to minimize leakage. As the minimum feature size of VLSI fabrication processes continues to shrink with each successive process generation along with the value of supply voltage and therefore the threshold voltage of the devices, leakage currents increase exponentially. Leakage currents are hence seen as a necessary evil in traditional VLSI design methodologies. We present an approach to turn this problem into an opportunity. In the second study in this dissertation we attempt to exploit leakage currents to perform computation. We use sub threshold digital circuits and come up with ways to get around some of the pitfalls associated with sub threshold circuit design. These include a technique that uses body biasing adaptively to compensate for Process Voltage and Temperature (PVT) variations, a design approach that uses asynchronous micro pipelined Network of Programmable Logic Arrays (NPLAs) to help improve the throughput of sub threshold designs, and a method to find the optimum supply voltage that minimizes energy consumption in a circuit.

Ubiquitous Computing Application and Wireless Sensor James J. (Jong Hyuk) Park, Yi Pan, Han-Chieh Chao, Gangman Yi, 2015-03-04 IT changes everyday's life especially in education and medicine

The goal of ITME 2014 is to further explore the theoretical and practical issues of Ubiquitous Computing Application and Wireless Sensor Network. It also aims to foster new ideas and collaboration between researchers and practitioners. The organizing committee is soliciting unpublished papers for the main conference and its special tracks. **Transition of HPC Towards Exascale Computing** Erik H. D'Hollander, Jack J. Dongarra, Ian Foster, Lucio Grandinetti, 2013-10-15. The US, Europe, Japan, and China are racing to develop the next generation of supercomputers: exascale machines capable of 10 to the 18th power calculations a second by 2020. But the barriers are daunting: the challenge is to change the paradigm of high performance computing. The 2012 biennial high performance workshop held in Cetraro, Italy, in June 2012 focused on the challenges facing the computing research community to reach exascale performance in the next decade. This book presents papers from this workshop arranged into four major topics: energy scalability, new architectural concepts, and programming of heterogeneous computing systems. Chapter 1 introduces the status of present supercomputers, which are still about two orders of magnitude separated from the exascale mark. Chapter 2 examines energy demands, a major limiting factor of today's fastest supercomputers; the quantum leap in performance required for exascale computing will require a shift in architectures and technology. In Chapter 3, scalable computer paradigms for dense linear algebra on massive heterogeneous systems are presented, and Chapter 4 discusses architectural concepts. Finally, Chapter 5 addresses the programming of heterogeneous systems. This book will be of interest to all those wishing to understand how the development of modern supercomputers is set to advance in the next decade.

Advances in Computer Systems Architecture Chris Jesshope, 2006-08-31. This book constitutes the refereed proceedings of the 11th Asia Pacific Computer Systems Architecture Conference (ACSAC 2006). The book presents 60 revised full papers together with 3 invited lectures addressing such issues as processor and network design, reconfigurable computing, and operating systems, and low level design issues in both hardware and systems. Coverage includes large and significant computer based infrastructure projects, the challenges of stricter budgets in power dissipation, and more.

Embedded Computer Systems: Architectures, Modeling, and Simulation Stamatis Vassiliadis, Stephan Wong, Timo D. Hämäläinen, 2006-07-18. This book constitutes the refereed proceedings of the 6th International Workshop on Systems Architectures, Modeling, and Simulation (SAMOS 2006) held in Samos, Greece, on July 2006. The 47 revised full papers presented together with 2 keynote talks were thoroughly reviewed and selected from 130 submissions. The papers are organized in topical sections on system design and modeling, wireless sensor networks, processor design, dependable computing, architectures and implementations, and embedded sensor systems.

Proceedings of ASP-DAC/VLSI Design 2002, 2002. Papers from a January 2002 conference are organized into four sessions, each on low power design, synthesis, testing, layout, and interconnects, and technology, as well as two sessions each on embedded systems verification and VLSI architecture, one session on analog design, and one session on hot c.

Proceedings of the ... ACM Great Lakes Symposium on VLSI, 2007. **High Performance Techniques for Reducing Cache Power** Major Balram

Bhadauria,2008 **Low-Power High-Level Synthesis for Nanoscale CMOS Circuits** Saraju P. Mohanty,Nagarajan Ranganathan,Elias Kougiannos,Priyadarsan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits *SIGMETRICS '07* ,2007

Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies Stephan Henzler,2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side Tutorial Guide ,2003 This text covers topics including leading edge packaging technology Pb free interconnections quality and reliability issues of portable products high density substrates and

embedded components and leaded and lead free solder characterization and modelling *CASES ...* ,2003 ISLPED'04
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Lee,2001 *IEICE Transactions on Electronics* ,2008 **Proceedings** ,2004 GLSVLSI '05 ,2005

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