- Adder
- Comparator
- Logic gates
- Multiplexers

S_1S_0	Action	Output
00	Load	$b_3b_2b_1b_0$
01	Keep current value	A
10	if(B>A) Load B/2; else Load B*2	if(B>A) B/2; else B*2
11	if(B<A/2) Load B; else keep current value	if(B<A/2) B; else A

13.   From the following state diagram, create the state table, and corresponding circuit using D flip–flops.
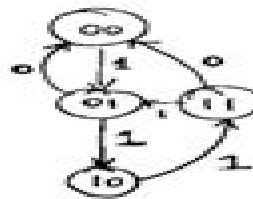
14.   Design a counter which cycles through the binary sequence (1, 2, 4, 5, 6, 7) using J/K flipflops. Show that when states 000 and 011 are used as don't care statements the counter may not operate properly. Suggest how to correct this problem.

15.   Design an arithmetic circuit with two selection variables, s1 and s0 that generates the following arithmetic operations.

Draw the logic diagram of one typical stage.

S1	S0	$C_{in} = 0$	$C_{in} = 1$
0	0	F = A	F = A + 1
0	1	F = A − B - 1	F = A - B
1	0	F = B − A - 1	F = B - A
1	1	F = A + B	F = A + B + 1

16.   Design one stage accumulator for the following operations:

Addition, Subtraction, Increment.

⇔⇔⇔

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