



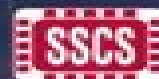
ISSCC 2026 CALL FOR PAPERS

IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

SUNDAY-THURSDAY, FEBRUARY 15-19, 2026

SAN FRANCISCO MARRIOTT MARQUIS, SAN FRANCISCO, CA

ISSCC WEBSITE: <http://isscc.org>



ISSCC 2026 CONFERENCE THEME: ADVANCING AI WITH IC & SoC INNOVATIONS

ISSCC is in the 73rd year as the flagship conference for solid-state circuit design. ISSCC promotes and shares new circuit and system ideas with the potential to advance the state-of-the-art in integrated-circuit (IC) and system-on-chip (SoC) designs. This year's conference theme highlights how today's circuit and system research and development contribute to IC and SoC innovations for advancing current and future artificial intelligence (AI) systems.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Circuits with analog-dominated innovation: amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally assisted analog circuits; sensor interface circuits; MEMS sensor/actuator interfaces; analog circuits in sub-10nm scaled technologies.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; time-to-digital converters. Focus is on innovative and emerging converter architectures and the integration advantages within larger systems, rather than the figure of merit (FoM) of isolated converters. Submissions should consider converter peripherals, such as input, reference, and clock drivers. Calibration techniques should focus on innovation, robustness, and practical usability.

DIGITAL CIRCUITS, ARCHITECTURES, & SYSTEMS^{*}:** Digital circuits, building blocks, and architectures with hardware (HW) optimization of complete systems (monolithic, chiplets, 2.5D, and 3D) for microprocessors, micro-controllers, application processors, graphics processors, automotive processors, processors for machine learning (ML) and artificial intelligence (AI), and system-on-chip (SoC) processors. Digital systems and accelerators for communications, video, and multimedia, cloud and datacenter applications, optimization processors and accelerators, reconfigurable systems, near- and sub-threshold systems, and emerging applications. Digital circuits and architectures for intra-chip communication, clock distribution, soft-error, and variation-tolerant design, power management (e.g., voltage regulators, adaptive digital circuits, digital sensors), and digital clocking circuits (e.g., PLLs, DLLs) for processors. Digital circuits and systems, including near-memory and in-memory computation and HW optimizations for new ML models, such as transformers, graph and spiking neural networks, and hyper-dimensional computing.

IMAGE SENSORS & DISPLAYS^{*}:** Image sensors; vision sensors, including event-based and computer sensors; LiDAR, time-of-flight, and depth sensing; machine learning and edge computing for imaging applications; display drivers, touch sensing, haptic displays, and interactive display and sensing technologies for AR/VR.

MEDICAL^{*}:** Medical devices; biomedical sensors and SoCs; brain-computer interfaces, neural interfaces, and closed-loop systems; wearable, implantable, and ingestible devices; ultrasound and medical imaging; medical optical microsystems; body area networks; wireless power transfer and communication to implantable devices; machine learning and edge computing for medical applications; combinatorial innovation, including sensor fusion for disruptive clinical outcomes.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces for memories; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power, reliability, performance, and fault tolerance; application-specific circuit enhancements within the memory subsystem; in-memory-computing and near-memory-computing macros for AI or other applications.

POWER MANAGEMENT: Power management, power delivery, and control circuits; switched-mode power converter ICs using inductive, capacitive, piezoelectric, and hybrid techniques; LDO/linear regulators; power delivery for heterogeneous integrated systems, and 2.5/3D-heterogeneous integrated power delivery; gate drivers; wide-bandgap (GaN/SiC) designs; isolated and wireless power converters; envelope supply modulation; energy-harvesting circuits and systems; power-management circuits for automotive and other harsh environments, robotics, LED drivers, and LiDAR.

RF CIRCUITS & WIRELESS SYSTEMS^{*}:** Complete solutions and building blocks at RF, mm-Wave, and THz frequencies for receivers, transmitters, frequency synthesizers, RF filters, transceivers, SoCs, and wireless SiPs incorporating multiple chiplets. Innovative circuits, systems, design techniques, heterogeneous packaging solutions, etc. for established and emerging wireless standards as well as future systems or novel applications, such as sensing, radar, imaging, satellite communications, and those improving spectral and energy efficiency.

SECURITY: Chips demonstrating cryptographic accelerators, smart-card security, trusted/confidential computing, security circuits (e.g., PLUFs, TRNGs, side-channel and fault-attack countermeasures, circuits and sensors for attack detection and prevention), security for resource-constrained systems, secure micro-processors, secure memories, analog/mixed-signal circuit security (e.g., secure ADC/DAC, RF, sensors), secure supply chains (e.g., hardware trojan countermeasures, trusted microelectronics), security for/with emerging technologies, core circuit-level techniques for logical/physical-level security, secure system integration for specific applications, and secure design methodologies.

TECHNOLOGY DIRECTIONS: Emerging and novel IC, system, and device solutions in various areas, such as integrated photonics, silicon electronics-photonics integration, quantum devices for metrology, sensing, computing, etc.; flexible, stretchable, foldable, printable, and 3D electronic systems; biomedical sensors for cellular and molecular targets; wireless power transfer at-distance (e.g., RF and mm-wave, optical, ultrasonic); ICs for space applications and other harsh environments; novel and unconventional platforms for computing and machine learning, including analog and mixed signal techniques; integrated meta-materials, circuits in alternative device platforms (e.g., carbon, organic, superconductor, spin, etc.). Chip-scale autonomous microsystems and microrobots.

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, copper-cable links, chip-to-chip communications, die-to-die interconnects, on-chip/on-package links, high-speed interfaces for memory, optical links and silicon photonics; exploratory I/O circuits for advancing data rates, bandwidth density, power efficiency, equalization, robustness, and design methodologies; building blocks for wireline transceivers, such as AGCs, analog frontends, ADC/DAC/DSPs, TIAs, equalizers, clock generation and distribution circuits, including PLLs/DLLs, clock recovery, line drivers, and hybrids.

^{*}This category will be reviewed by either the Digital Circuits Subcommittee or the Digital Architectures & Systems Subcommittee.

^{**}The ISSCC 2025 Imaging, Medical, & Display Subcommittee has been separated into the Image Sensors & Displays Subcommittee and the Medical Subcommittee.

^{***}This category will be reviewed by either the RF Subcommittee or the Wireless Subcommittee.

Deadline for Electronic Submission of Papers:

Wednesday, September 3, 2025 • 3:00 PM Eastern Daylight Time (19:00 GMT)

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10th International Symposium on Asynchronous Circuits and Systems ,2004 IEEE Computer Society Order Number P2133 T p verso **ICASSP 86** ,1986 **Applied Reconfigurable Computing. Architectures, Tools, and Applications** Fernando Rincón,Jesús Barba,Hayden K. H. So,Pedro Diniz,Julián Caba,2020-03-25 This book constitutes the proceedings of the 16th International Symposium on Applied Reconfigurable Computing ARC 2020 held in Toledo Spain in April 2020 The 18 full papers and 11 poster presentations presented in this volume were carefully reviewed and selected from 40 submissions The papers are organized in the following topical sections design methods design space exploration high level synthesis architectures applications **Proceedings, International Test Conference 1996** ,1996 ITC is the World s largest premier technical conference on the testing and total quality of integrated electronics and the assenblies and systems that are based on them ICASSP 85 ,1985 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1996 Issues for 1973 cover the entire IEEE technical literature **IEICE Transactions on Electronics** ,1999

1986 IEEE International Symposium on Circuits and Systems, Le Baron Hotel, San Jose, California, May 5-7, 1986 ,1986

IEICE Transactions on Communications, Electronics, Information, and Systems ,1991 **Proceedings - Compcon** ,1984 **IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis** ,2005 **CODES+ISSS** ,2005 **ISSCC 79** IEEE Solid-State Circuits Council,1979

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